Amendments to the Claims

Claim 1 **(Previously Presented)** A receiver for detecting an approximate value of the power of a reception signal, the receiver comprising:

first operation means for adding a value obtained by multiplying a smaller one of a component I and a component Q of the reception signal by 1/8 and a value of a larger one of the components I and Q;

second operation means for adding a value obtained by multiplying the smaller one of the component I and the component Q of the reception signal by 1/2 and a value obtained by multiplying the larger one of the components I and Q by 7/8; and

detection means for detecting a value of a larger one of an operation result of said first operation means and an operation result of said second operation means as the approximate value of the power of the reception signal.

Claim 2 **(Previously Presented)** A receiver for detecting an approximate value of the power of a reception signal, the receiver comprising:

a first comparator for comparing a component I and a component Q of the reception signal with each other to determine which one of the components I and Q is larger or smaller to thereby output a larger component as a first output value and output a smaller component as a second output value;

a 3-bit shift register for multiplying the first output value from said first comparator by 1/8;

a subtractor for subtracting an output value from said 3-bit shift register from the first output value from said first comparator;

a 1-bit shift register for multiplying the second output value from said first comparator by 1/2;

a 2-bit shift register for multiplying an output value from said 1-bit shift register by 1/4;

a first adder for adding the first output value from said first comparator and an output value from said 2-bit shift register;

a second adder for adding an output value from said subtractor and the output value from said 1-bit shift register; and

a second comparator for comparing an output value from said first adder and an output value from said second adder with each other to determine which one of the output values is larger or smaller and output a value of a larger one thereof as the approximate value of the power of the reception signal.

Claim 3 **(Previously Presented)** A mobile-station device for detecting an approximate value of the power of a signal radio-received from a base-station device, the mobile-station device including a receiver comprising:

first operation means for adding a value obtained by multiplying a smaller one of a component I and a component Q of the reception signal by 1/8 and a value of a larger one of the components I and Q;

second operation means for adding a value obtained by multiplying the smaller one of the component I and the component Q of the reception signal by 1/2 and a value obtained by multiplying the larger one of the components I and Q by 7/8; and

detection means for detecting a value of a larger one of an operation result of said first operation means and an operation result of said second operation means as the approximate value of the power of the reception signal.

Claim 4 **(Previously Presented)** A mobile-station device for detecting an approximate value of the power of a signal radio-received from a base-station device, the mobile-station device including a receiver comprising:

a first comparator for comparing a component I and a component Q of the reception signal with each other to determine which one of the components I and Q is larger or smaller to thereby output a larger component as a first output value and output a smaller component as a second output value;

a 3-bit shift register for multiplying the first output value from said first comparator by 1/8;

a subtractor for subtracting an output value from said 3-bit shift register from the first output value from said first comparator;

a 1-bit shift register for multiplying the second output value from said first comparator by 1/2;

a 2-bit shift register for multiplying an output value from said 1-bit shift register by 1/4;

a first adder for adding the first output value from said first comparator and an output value from said 2-bit shift register;

a second adder for adding an output value from said subtractor and the output value from said 1-bit shift register; and

a second comparator for comparing an output value from said first adder and an output value from said second adder with each other to determine which one of the output values is larger or smaller and output a value of a larger one thereof as the approximate value of the power of the reception signal.

Claim 5 **(Previously Presented)** A detection method for detecting an approximate value of the power of a signal received from a receiver, the detection method comprising:

adding a value obtained by multiplying a smaller one of a component I and a component Q of the reception signal by 1/8 and a value of a larger one of the components I and Q to set an addition result as a first operation result;

adding a value obtained by multiplying the smaller one of the component I and the component Q of the reception signal by 1/2 and a value obtained by multiplying the larger one of the components I and Q by 7/8 to set an addition result as a second operation result; and

detecting a value of a larger one of the first operation result and the second operation result as the approximate value of the power of the reception signal.

Claim 6 **(Previously Presented)** A detection method for detecting an approximate value of the power of a signal received from a receiver, the detection method comprising:

comparing a component I and a component Q of the reception signal with each other to determine which one of the components I and Q is larger or smaller through operation of a first comparator, to thereby output a larger component as a first output value and output a smaller component as a second output value;

multiplying the first output value from the first comparator by 1/8 through operation of a 3-bit shift register;

subtracting an output value from the 3-bit shift register from the first output value from the first comparator through operation of a subtractor;

multiplying the second output value from the first comparator by 1/2 through operation of a 1-bit shift register;

multiplying an output value from the 1-bit shift register by 1/4 through operation of a 2-bit shift register;

adding the first output value from the first comparator and an output value from the 2-bit shift register through operation of a first adder;

adding an output value from the subtractor and the output value from the 1-bit shift register through operation of a second adder; and

comparing an output value from the first adder and an output value from the second adder with each other through operation of a second comparator, to thereby determine which one of the output values is larger or smaller and detect a value of a larger one thereof as the approximate value of the power of the reception signal.

Claims 7 and 8 **(Canceled)**

Claim 9 **(Previously Presented)** A detection method for detecting and outputting an approximate value of the power of a signal received from a receiver, the detection method comprising:

performing a plurality of operations using a plurality of approximate equations that are different from each other and each include at least one bit shift operation, at least one add or subtract operation and at least one compare operation, to calculate from the same reception signal a plurality of candidates for the approximate value of the power of the reception signal; and

detecting an excellent candidate from among the plurality of candidates as the approximate value of the power of the reception signal to outputted.